

Enhanced FPGA-Based Controller for Three Phase Shunt Active Power Filter

Research paper

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Abstract: In this paper, a three-phase shunt active power filter (SAPF) controller with a fully digital implementation is presented. The main goal of this contribution is to implement a digital direct power control (DDPC) algorithm without phase-locked-loop (PLL) for SAPF. This algorithm is intended for power quality improvement and current harmonic elimination. The controller introduced in this paper is cost-effective, has a fast-dynamic response, and has a simple hardware implementation. In order to comply with the above specifications, a dedicated controller has been conceived and fully implemented within a field-programmable gate array (FPGA) device. This FPGA-based controller integrates the whole signal-processing functions needed to drive the SAPF, as well as an original method for sector identification. The intended controller provides the desired power references to select the optimal switching sequences. The switching orders follow the grid reference to drive the voltage source inverter (VSI), so the SAPF achieves good performances while ensuring balanced overall supply currents, unity power factor, and reduced harmonic load currents. The proposed digital implementation achieves a valuable compromise between fast dynamic response, minimum execution time, and reduced FPGA resources, through a simple hardware design implementation. The entire system is developed and simulated using VHDL and VHDL-AMS languages.

Keywords: Shunt active power filter • direct power control • harmonic elimination • reactive power compensation • field-programmable gate array

1. Introduction

In electric power distribution systems, reactive power and harmonic current cause hazardous problems, such as line losses, transformer overheating, interfering with adjacent communication networks, and disturbing sensitive loads (Mikkili and Panda, 2018; Singh et al., 1999). Active power filters (APFs), especially, shunt active filters (SAPFs), have been considered as an effective solution for these issues. APF can compensate harmonic current by continuously tracking the changes in harmonic contents, to finally reshape the source current to the sinusoidal form (Li et al., 2021).

Nowadays, several control strategies and schemes for APF are proposed and studied (Akagi, 2005; Baros et al., 2022; Jain, 2018; Li et al., 2021; Montero et al., 2007; Singh et al., 1999; Zahira and Fathima, 2012). The main idea of the control strategy for APF is to calculate the reference current that must be delivered by a voltage source inverter (VSI) to compensate instantaneous reactive power and to eliminate the harmonic current.

The deterioration of the grid quality is due to non-linear loads that are connected to the grid. Controlling APF involves a set of measurements to generate the switching signals applied to the VSI by means of an appropriate closed-loop switching control technique such as dead-beat or hysteresis control.

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To be efficient, APF control strategies are digitally implemented. However, it is very difficult to adapt these control strategies for the realisation of digital implementations (Shu et al., 2008), especially in a high-sampling-rate system with limited computational resources. Microprocessors, microcontrollers, and digital signal processors (DSP) have been largely used for implementation of an APF controller in a discrete-time environment (Anjana et al., 2016; Dash and Ray, 2017; Garcia-Cerrada et al., 2007; Mulla et al., 2015; Popescu et al., 2012; Singh et al., 2000; Yu et al., 2020). To reduce the computational effort of a digital controller and to reduce time-delays and processing latency, the field-programmable gate array (FPGA) is largely dominating (Karimi et al., 2008; Sharma et al., 2019; Shu et al., 2008; Sundaram and Venugopal, 2016).

Generally, FPGA is used when we need fast processing and parallel computing; they are also a good support for rapid prototyping, thanks to their reconfigurable capability that can considerably enhance the system design and system deployment (Monmasson et al., 2011; Rodriguez-Andina et al., 2007). All these features make FPGA a good choice for high-speed processing algorithms in digital applications and industrial control systems. On the other hand, all control strategy requirements do not match with FPGA device resources and limitations, so our work is focused on developing the digital adaptation of a widely used control strategy to be refined and implemented in the FPGA device.

Direct power control (DPC) strategy was used in this paper owing to its effectiveness and simplistic structure. DPC is based on the control of instantaneous active and reactive power using a nonlinear control loop. In DPC there is no need for an internal current regulator, no need for a phase-locked loop (PLL) generator, and no pulse modulation block (PWM) is required (Noguchi et al., 1998).

Therefore, the important point for the employment of a DPC is a precise and fast approximation of the active and reactive line power. DPC consists in selecting the switching state of the power converter from a referenced look-up table; these states are based on calculating instantaneous errors of active and reactive powers as well as the angular position of the expected grid voltage vector (Sharma et al., 2019). These features make DPC an ideal technique for implementation on medium-sized FPGAs.

In this context, the paper presents an enhanced digital DPC controller designed for FPGA implementation. An effective way to design is used to improve each part of the controller individually, then assembled in an efficient model to reach the design objectives. The main contribution of this paper is the design of an improved controller in terms of FPGA resources saving and dynamic response speed, balanced with good operating performances. To achieve these goals, the controller parts are modelled with the purpose of avoiding the use of CORDIC algorithms, which are resource-intensive. Then a binary representation of all variables involved in the controller is adopted. After several verifications, this data format is considered in order to reduce the hardware resources while assuming acceptable performance. Taking into consideration the above-mentioned points, hardware resources are reduced and consequently decrease time propagation in FPGA processing elements. Finally, with adequate dataflow synchronisation, global optimisation of the controller operation is reached.

This paper is organised as follows. After an introduction, Section 2 introduces a presentation of the DPC strategy for active power filtering. Sections 3 and 4 describe the hardware implementation of the digital DPC on the FPGA device. Then, Section 5 presents the most important elements of software simulations using VHDL-AMS language, to show the benefits and effectiveness of our approach. The last section states the conclusion and summarises the most salient features of our contribution.

2. The Principle of DPC for SAPF

DPC is used in a versatile application where a grid-connected inverter is needed. It is based on evaluation of the active and reactive instantaneous power error values and the grid voltage vector position without any internal control loop for the currents (Bouafia et al., 2012; Noguchi et al., 1998).

There are a variety of DPC schemes in the literature (Bouafia et al., 2009; Hu et al., 2011; Mesbahi et al., 2014; Nian et al., 2015; Vazquez et al., 2015; Yan et al., 2021; Zhi et al., 2009) and the most used for SAPF control is the well-known look-up-table (LUT) DPC (Alonso-Martinez et al., 2010). The block diagram depicted in Figure 1 shows the typical LUT-DPC configuration applied for SAPF control.

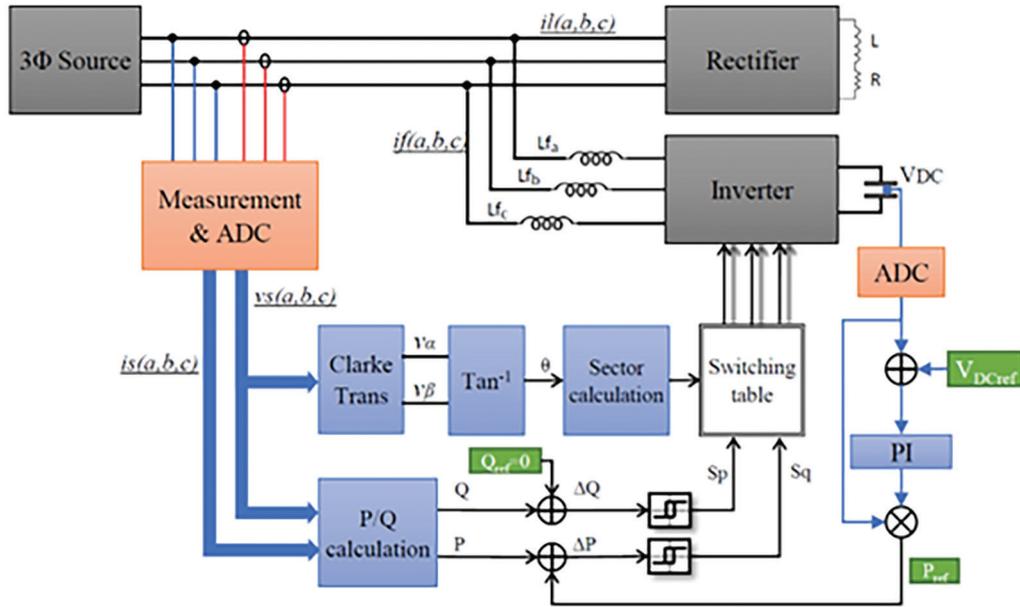


Fig. 1. General scheme of DPC applied for shunt APF. ADC, analog-to-digital converter; APF, active power filter; DPC, direct power control.

The first step to achieve DPC for an SAPF system is to measure the three-phase grid voltage and line current, and then to determine the instantaneous active power and reactive power according to Eqs (1) and (2):

$$p_s(t) = v_{sa} \cdot i_{sa} + v_{sb} \cdot i_{sb} + v_{sc} \cdot i_{sc} \quad (1)$$

$$q_s(t) = \frac{1}{\sqrt{3}} \left[(v_{sa} - v_{sb}) \cdot i_{sa} + (v_{sb} - v_{sc}) \cdot i_{sb} + (v_{sc} - v_{sa}) \cdot i_{sc} \right] \quad (2)$$

The main idea of the DPC strategy is to activate a given state of a power inverter according to the evolution of the active and reactive power in time. This is done through the use of two hysteresis comparators with inputs as the error among the reference and the calculated values of the active and reactive power ΔP_s and ΔQ_s as expressed in Eqs (3) and (4):

$$\Delta P_s = P_{ref} - p_s(t) \quad (3)$$

$$\Delta Q_s = Q_{ref} - q_s(t) \quad (4)$$

Where P_{ref} is the active power reference (given from the DC bus voltage proportional-integral [PI] controller) and Q_{ref} is the reactive power reference ($Q_{ref} = 0$ to achieve unity power factor operation).

Passing over the hysteresis band is indicated with a logic state (S_p, S_q) that permits to select the next combination of activated inverter switch.

2.1. Clarke transformation

The influence of the evolution of the instantaneous active and reactive power is dependent on the direct position of the grid voltage vector. The angular position of the source voltage is transformed into a numerical signal θ_n . For this reason, the stationary coordinates are partitioned into 12 sectors, as shown in Figure 2.

$$(n-2)\frac{\pi}{6} < \theta_n \leq (n-1)\frac{\pi}{6} \quad n = 1, 2, \dots, 12 \quad (5)$$

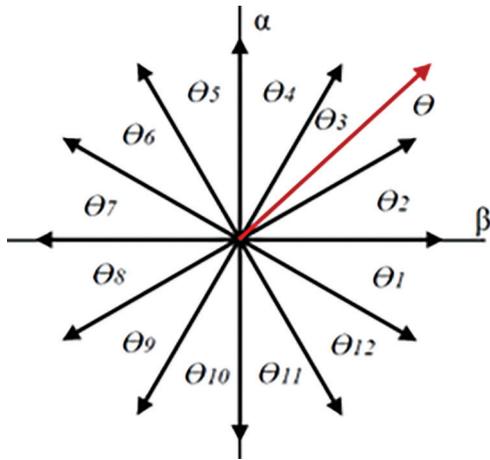


Fig. 2. Sectors and voltage vector on stationary coordinates.

The source voltage vector can be expressed on the stationary coordinates as:

$$v_{ab}(t) = \frac{2}{3} \begin{bmatrix} 1 & \frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \quad (6)$$

2.2. Switching table-based DPC

To command directly the VSI transistors, the sequence of every switching state 'Sa, Sb, Sc' is retrieved from a two-dimension table (see Table 1). The sequence is selected according to the value of the input signals S_p , S_q , and the phase θ_n . The selection of the switching state is achieved to make the active power and reactive power variations kept inside the hysteresis bands.

S_p	S_q	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
1	0	101	111	100	000	110	111	010	000	011	111	001	000
	1	111	111	000	000	111	111	000	000	111	111	000	000
0	0	101	100	100	110	110	010	010	011	011	001	001	101
	1	100	110	110	010	010	011	011	001	001	101	101	100

Table 1. Switching table for direct instantaneous power control.

2.3. DC voltage PI controller

In order to reduce the variations of the DC-link capacitor voltage and to maintain it at the required level, a PI controller is used, where the controller input is the difference between the DC-link voltage V_{DC} and the reference value V_{DCref} , the controller output signal is then multiplied by V_{DC} to provide the estimation of the instantaneous active power reference P_{ref} where:

$$P_{ref} = V_{DC} * I_{max} \quad (7)$$

3. Digital DPC for FPGA Implementation

In such design, it is important to follow a model-based design approach, where each module of the system is designed and optimised individually to execute a specific task. This may increase the possibility of reusing and evolving these modules for future implementations in similar applications.

The full architecture has been implemented in FPGA devices using Avnet Spartan-6 LX9 MicroBoard, a low-cost FPGA board that operates at 100 MHz and has sufficient resources to embed complex power electronics controller as it operates at a medium-high frequency.

Fixed-point arithmetic has been used to carry out the hardware design, the choice of word sizes, and the binary format is very important. All input variables are coded in a signed format with a word size of 16 bits, and internal variables are coded in different formats depending on the desired accuracy and according to the available FPGA resources.

The present DPC controller consists of six independent modules as illustrated in Figure 3. In addition, a supervisor block manages the different controller tasks and ensures that the switching signals are applied simultaneously during every sampling period. In order to obtain optimal performance for active power filtering, DPC should be performed at high-processing speed, which can be successfully accomplished by using an FPGA device; however, in FPGA applications, trigonometric functions and square root operation can have a bad impact on the performance of the whole system, due to their complex implementation.

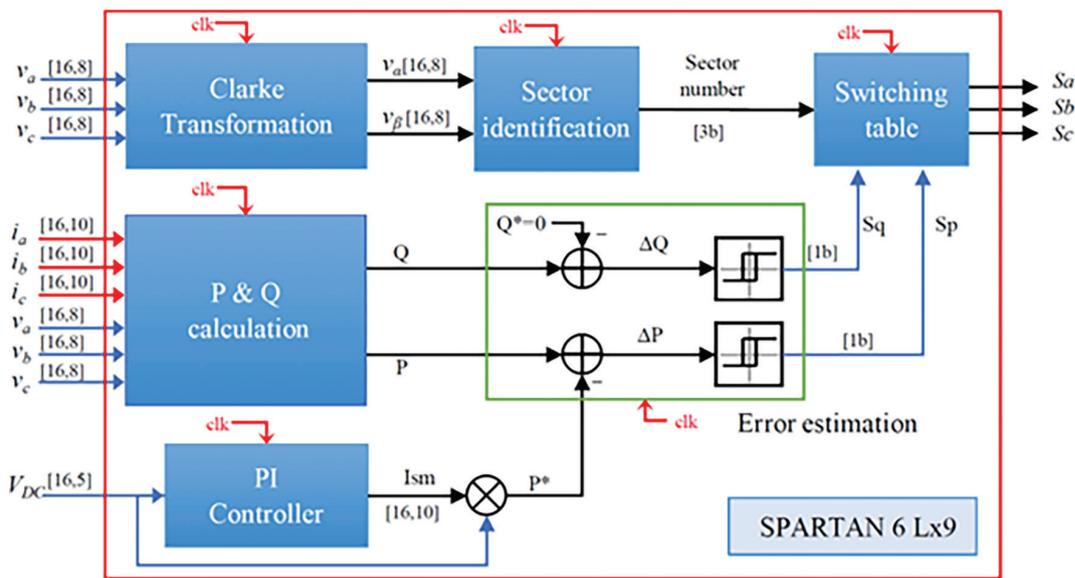


Fig. 3. The hardware architecture of the digital DPC controller. DPC, direct power control; PI, proportional-integral.

This section presents the description of each module and its implementation in the above-mentioned FPGA. The hardware architecture consists of six functional blocks that are developed from the different steps of the DPC strategy specified in Section 2. These operational blocks are described below.

3.1. P & Q calculation block

Active power and reactive power are directly calculated from the three-phase instantaneous current and voltage using Eqs (1) and (2). The variables are converted from analog to digital format, where an adequate binary representation is used for each variable. As aforementioned, the voltage and current variables have a 16 bit length in two's complement fixed-point format [16.8b] and [16.10b], respectively. So, in the present work, the voltage does not exceed ± 127 V and the current does not exceed ± 32 A. Respecting these values and the system scheme, the active and reactive power are represented in [24.10b] format.

3.2. PI controller

The discrete-time domain approximation of a PI controller is given by Eq. (8), where the controller output ($u[k]$) flow is evaluated from the error between the DC-link capacitor voltage V_{DC} and the reference V_{DCref} :

$$u[k] = u[k-1] + K_1 e[k] + K_2 e[k-1] \quad (8)$$

where $K_1 = K_p + Ts K_i$, $K_2 = -K_p$, and Ts is the sampling period.

The two parameters K_p and K_i represent the proportional and integrator gain coefficients derived from the analog form of the PI controller.

A simplified structure of the digital PI controller is presented in Figure 4; it shows the necessary FPGA elements required in the PI hardware implementation. where the coefficients K_1 and K_2 are expressed in signed [16.10b] digital format.

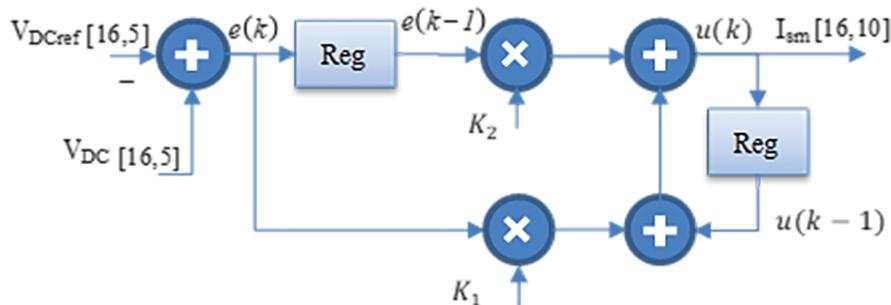


Fig. 4. Digital implementation of a PI controller. PI, proportional-integral.

3.3. Error estimation block

Three binary comparators of 32 bits are used to achieve the implementation of the error estimator: one comparator is used to calculate the difference between the instantaneous active power and the estimated active power, and the two other comparators are used for the hysteresis block. The outputs are two logic signals with 1 bit length S_q and S_p .

3.4. Clarke transformation block

The function of this module is to transform the stator phase voltage v_a , v_b , and v_c into the stationary coordinates v_α and v_β using Clarke transformation; refer to Eq. (6). The Clarke transformation module can be implemented on FPGA using the model presented in Figure 5; this configuration is optimised to reduce resources and make processing faster, by using a binary adapted format, and simpler Register Transfer Level (RTL) functions such as Left Shift (LS) operation.

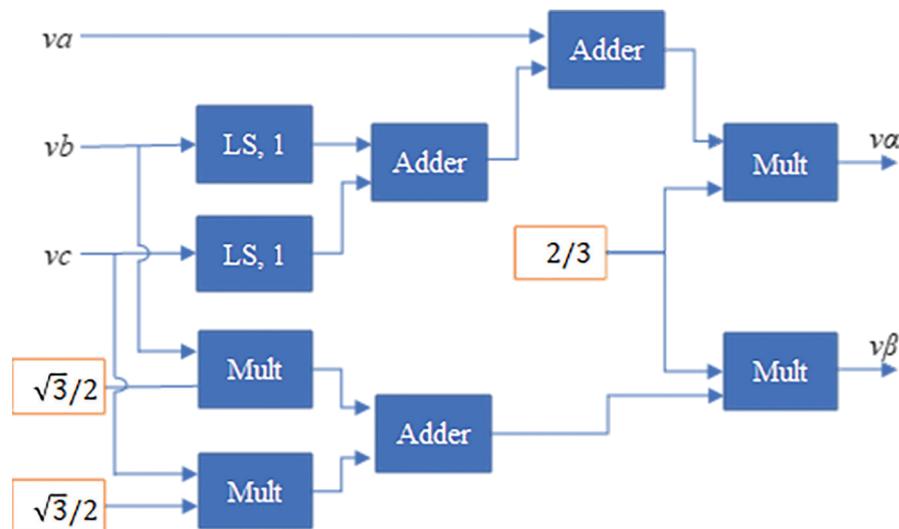


Fig. 5. Simplified digital implementation of Clarke transformation.

In this scheme, the values $\sqrt{3}/2$ and $2/3$ are represented in 8 bits format; this format is quite sufficient for this implementation. Therefore, $\sqrt{3}/2$ is represented as 0b11011110, and $2/3$ is represented as 0b10101011. The outputs

of this block (v_α and v_β) are truncated to 16 bits. Several verifications have been done to get a suitable data format that minimises hardware resources and maintains acceptable precision.

3.5. Sector identification block

The present work introduces a simple method to determine the sectors of the voltage vector, which is modified from Sutikno et al. (2010), and dedicated to digital implementation. The proposed method makes successive tests to identify the voltage vector position without using CORDIC algorithms.

The identification of the voltage sector depends on the location of the reference vector. In the voltage space vector, the reference vector is represented using its two components v_α and v_β . According to Table 2, first, the proposed algorithm determines in which quadrant the vector is placed by comparing v_α and v_β signs, then it determines the sector by comparing the vector tangent ($A = v_\alpha/v_\beta$) with $\tan(30^\circ)$ and $\tan(60^\circ)$.

Quadrant conditions	$A = v_\beta/v_\alpha$ condition	Angle interval	Sector	Code
Quadrant I $v_\alpha > 0$ and $v_\beta > 0$	$A < \sqrt{3}/3$	$[0, 30^\circ[$	02	0010
	$\sqrt{3}/3 < A < \sqrt{3}$	$[30^\circ, 60^\circ[$	03	0011
	$A > \sqrt{3}$	$[60^\circ, 90^\circ[$	04	0100
Quadrant II $v_\alpha < 0$ and $v_\beta > 0$	$A < \sqrt{3}/3$	$[90^\circ, 120^\circ[$	05	0101
	$\sqrt{3}/3 < A < \sqrt{3}$	$[120^\circ, 150^\circ[$	06	0110
	$A > \sqrt{3}$	$[150^\circ, 180^\circ[$	07	0111
Quadrant III $v_\alpha < 0$ and $v_\beta < 0$	$A < \sqrt{3}/3$	$[180^\circ, 210^\circ[$	08	1000
	$\sqrt{3}/3 < A < \sqrt{3}$	$[210^\circ, 240^\circ[$	09	1001
	$A > \sqrt{3}$	$[240^\circ, 270^\circ[$	010	1010
Quadrant IV $v_\alpha > 0$ and $v_\beta < 0$	$A < \sqrt{3}/3$	$[270^\circ, 300^\circ[$	011	1011
	$\sqrt{3}/3 < A < \sqrt{3}$	$[300^\circ, 330^\circ[$	012	1100
	$A > \sqrt{3}$	$[330^\circ, 360^\circ[$	01	0001

Table 2. Conditions for sector identification.

Where:

$$\tan(30^\circ) = \sqrt{3} \cong 1.732 \approx 1.10111011$$

$$\tan(60^\circ) = \sqrt{3}/3 \cong 0.57735 \approx 0.10010011$$

The last step of this algorithm is to code the sector number in 4 bits format to indicate the current vector position.

3.6. Switching table

The outputs of the sector identification module along with the state of the power status (S_q, S_p) are concatenated together in one binary sequence. This combination is used to generate the control signals (S_a, S_b, S_c) based on the switching states, which are stored on an embedded look-up table.

3.7. Timing and synchronisation

From Figure 3, it is obvious that the different DPC modules are interdependent and there is a sequence in which the operations have to be achieved. It is important to control effectively the data flow between these modules so that the system can work adequately and efficiently. All modules are activated by a sequence of control signals that are provided by a synchronous finite state machine (FSM). The FSM generates activating signals for each block within a fixed delay T_s (Sampling period), while the clock frequency is defined at 100 MHz. This sampling period is determined after taking into consideration the temporal limitations of the switching converter devices and the sampling step of the analog-to-digital converter (ADC).

Table 3 shows the time delays for each module of the digital DPC. The total delay time is obtained when all elements are connected in a sequential way.

Module	Path delay (ns)
Clarke transformation	17.14
Active and reactive power calculation	22.541
PI controller	6.483
Sector selection	194.37
Error estimation	12.465
Switching table	6.5
Total	259.5

DPC, direct power control; PI, proportional-integral.

Table 3. Time delay for each DPC module.

Taking advantage of the concurrent processing ability of FPGAs, the different blocks are connected together to achieve the appropriate data processing. Figure 6 shows the activation plan according to the required time per operation.

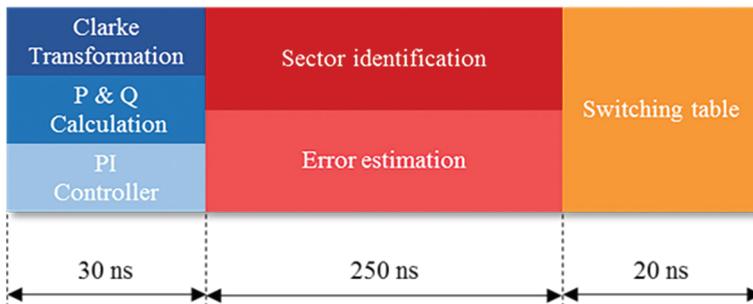


Fig. 6. Data path for digital DCP controller. DPC, direct power control.

At the beginning of each sample time step, and after the current and voltage measurements, the Clark transformation, power calculation, and PI control are executed in parallel within an operation period of 30 ns. In the next stage, the sector identification algorithm is performed in 250 ns in parallel with the error estimation module. Finally, the PWM signals are generated from the switching table within 20 ns.

4. FPGA Resources

Table 4 summarises the resource usage of all DPC elements, and the total resource-utilisation rate for the SPARTAN XC6SLX9 FPGA device, where the numbers of LUT slices and DSP slices are all individually tabulated.

Moreover, it is worth noting that with the considered hardware structure, the whole system can be synthesised using a medium-scale FPGA chip with only 3,383 LUT slices and 9 DSP slices used. This allows auxiliary modules to be implemented for further control techniques.

Module	Slice LUT	DSP
Clarke transformation	97	3
Active and reactive power calculation	1,230	3
PI controller	29	2
Sector selection	1,954	0
Error estimation	67	1
Switching table	6	0
Total	3,383	9
Rate	59% [5,720]	56% [16]

DSP, digital signal processors; FPGA, field-programmable gate array; LUT, look-up-table; PI, proportional-integral.

Table 4. FPGA resource utilisation.

5. Simulation Results

To evaluate the performance of the proposed control strategy for SAPF application under various operating scenarios, a detailed time-domain analysis is carried out via SMASH software from Dolphin Integration using VHDL-AMS and VHDL description language. These languages are used together to develop mixed-signal and digital applications. In a single simulation software, models are executed to enable verification and analysis of system dynamic behaviour. After that, the digital part, in this work a DPC controller, is implemented in an FPGA device using dedicated software with the intention to achieve hardware experiments (Benhamadouche et al., 2019).

For the purpose of simulation, the system parameters are listed in Table 5. Several test cases are applied to examine both the steady state and transient behaviour of the system. The main purpose of the simulation is to study three different aspects: (1) reactive power and harmonic currents compensation; (2) dynamic response of the system to current load variations; and (3) power factor correction.

Line voltage	100 V
Line frequency (f)	50 Hz
Filter inductance (L_{fa} , L_{fb} , L_{fc})	3 mH
DC bus capacitor (C)	2,600 μ F
Reference DC bus voltage (V_{DCref})	283 V
Nonlinear load (R, L)	5.1 Ω , 0.56 mH 10 Ω , 0.56 mH
Sampling frequency f_s	50 kHz

Table 5. System parameters.

5.1. Steady-state performance of the SAPF

The steady-state performance of the SAPF operating under the control of the proposed digital DPC implementation is shown in Figure 7, where a three-phase rectifier is coupled to the grid as a nonlinear load. In these waveforms, the load current, the compensating current, the source current, active and reactive power, and the DC-link capacitor voltage are displayed.

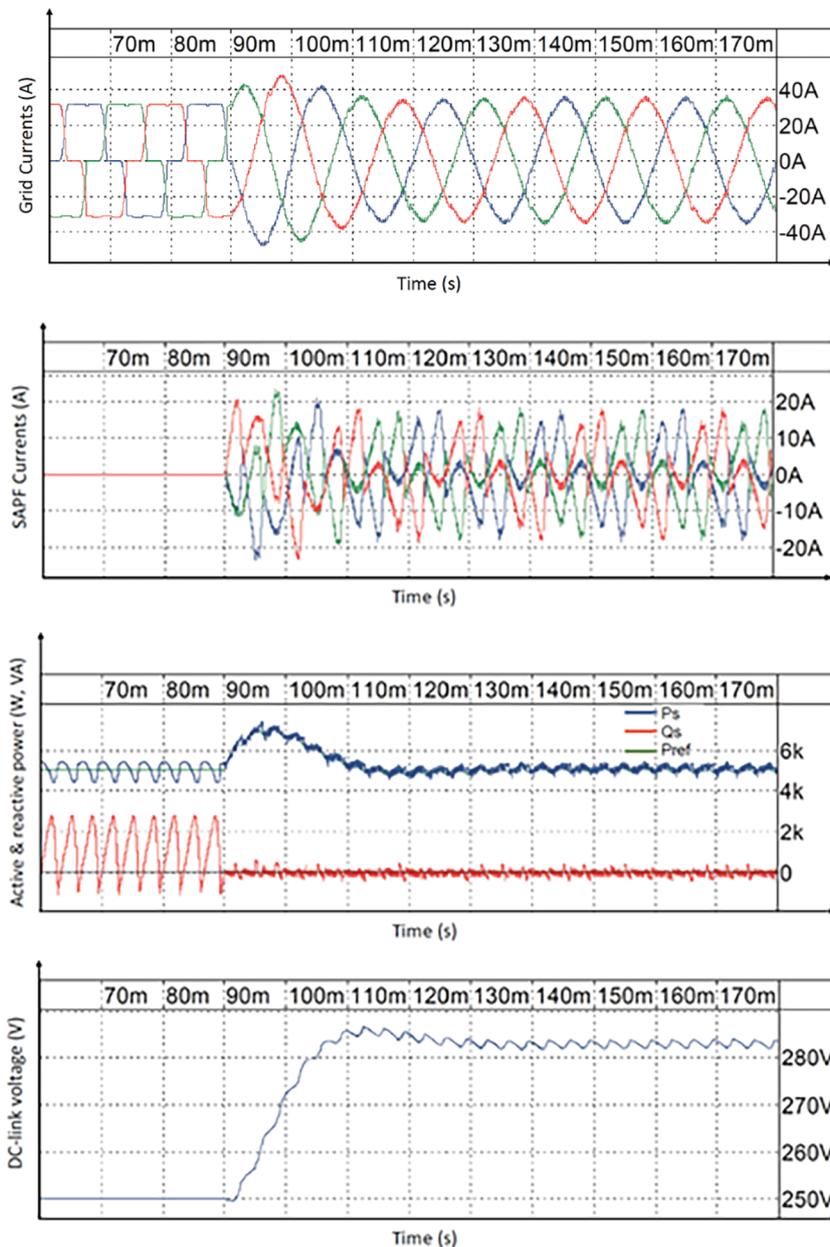


Fig. 7. Steady-state simulation results of SAPF using digital DPC, from top to bottom: Grid currents, SAPF current, active and reactive power, and DC-link capacitor voltage. DPC, direct power control; SAPF, shunt active power filter.

The three-phase source current is extremely distorted due to the current drawn by the nonlinear load. When the DPC controller is activated with the SAPF at $t = 90$ ms, the three-phase source current becomes sinusoidal. However, some amount of lower order harmonic is present in the source current, and the error is limited to 2 A. The THD of the source current can be brought down from 23.29% to 3.88% by compensation, well within the prescribed requirement limit of the IEEE 519 standard (5%). The DC-link capacitor voltage (V_{DC}) is successfully maintained around its reference value (V_{DCref}) with a very small ripple. Furthermore, the grid active power P_s is equal to 5020 W, and the grid reactive power Q_s is dragged from 1,200 VA to 0, showing that the proposed digital implementation of the DPC strategy is operational and effective.

5.2. Transient-state performance of the SAPF

Figure 8 shows the dynamic response of the SAPF running with the proposed controller, where a step increase and a step decrease of the load current are considered. The load variation is set by changing the load resistor value from $R = 5.1 \Omega$ to 10Ω at 100 ms and back from $R = 10 \Omega$ to 5.1Ω at 200 ms.

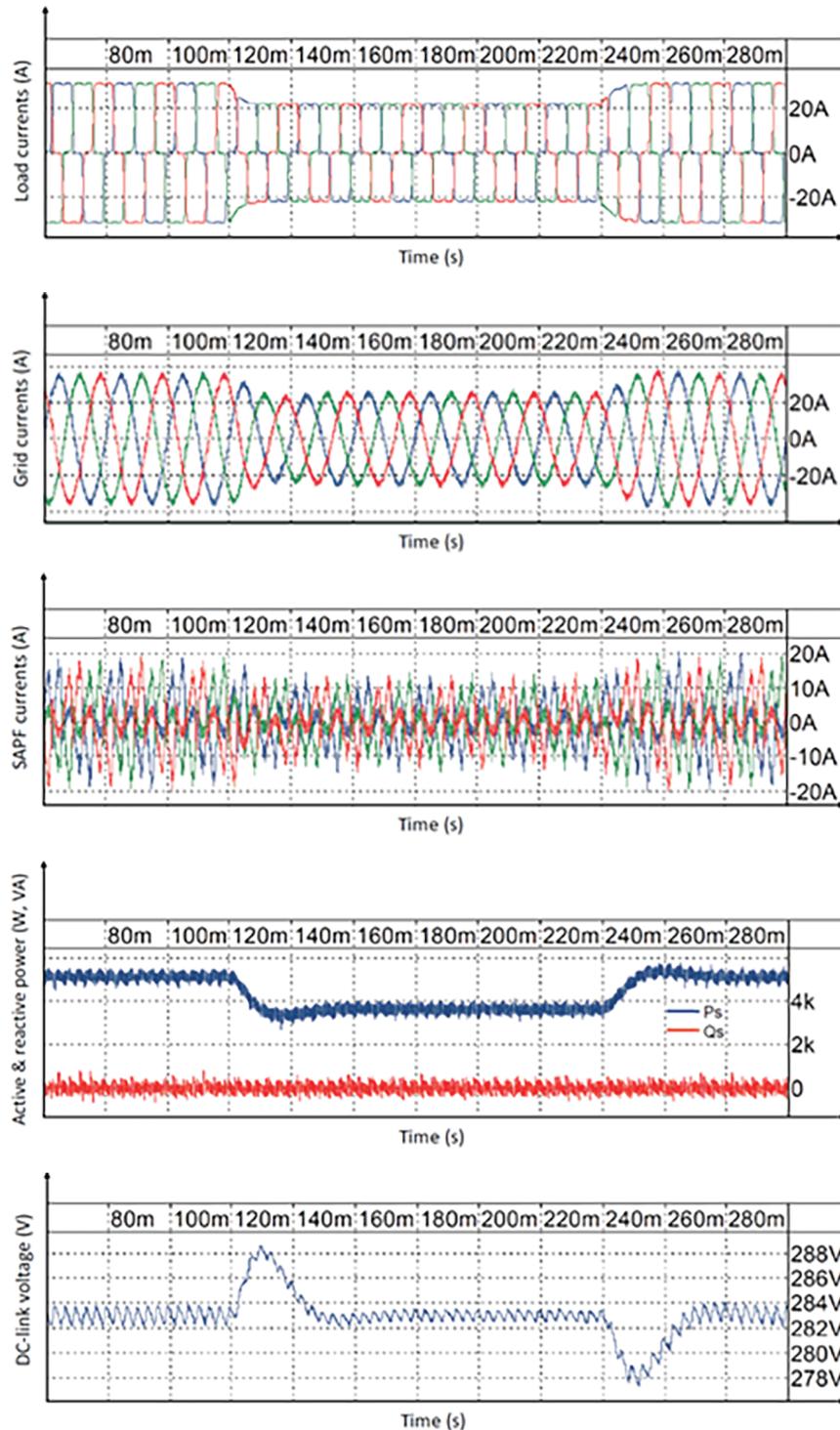


Fig. 8. Transient-state simulation results of SAPF using digital DPC, from top to bottom: Load currents, grid currents, SAPF currents, active power and reactive power and DC-link capacitor voltage. DPC, direct power control; SAPF, shunt active power filter.

The simulation results confirm that the proposed FPGA implementation is able to force the SAPF current to follow efficiently its reference when a change occurs on the grid current. A transient time of a one-and-a-half period was necessary for the current of the source to be almost balanced sinusoidal. Moreover, due to rapid variation of the nonlinear load current, the DC-link capacitor voltage (V_{DC}) oscillates similarly, which needs about one cycle and a half to attain its reference value (V_{DCref}). The same was true for active power, which changes according to the load needs, and the reactive power does not change and still follows its null reference. Furthermore, the voltage overshoot of the DC-link voltage is about 5.5 V; it does not exceed 2% of V_{DCref} in the transient-state, which shows the effectiveness of the digital implementation of the PI controller.

5.3. THD analysis

In this analysis, the SAPF system was examined with different load values. The grid current THD before compensation and after compensation is shown in Table 6. From the results, it is observed that the proposed controller offers better performance in most cases. Regarding the case with a large resistor value, the current drawn from the grid is smaller and the perturbation is proportionally more significant. This implies more effort from the SAPF to eliminate harmonics current. Moreover, in the elaborated controller the data format choice impacts also the performance of the SAPF. Therefore, a smaller load current needs a controller binary format with greater precision.

Scenarios (R load)	2.5 Ω	5.1 Ω	R = 10 Ω
THD with-out SAPF (%)	21.2	23.9	31.5
THD with SAPF (%)	3.16	3.88	5.05
Grid current fundamental with SAPF (A)	63.3	33.9	14.95

SAPF, shunt active power filter.

Table 6. Summary of THD analysis.

6. Conclusions

In this paper, a digital implementation for active power filtering is presented. This implementation uses DPC scheme and is run on a low-cost FPGA device; this implementation is intended to achieve a high-performance power control and current grid filtering.

All modules of the system were designed with a generic VHDL description, regardless of the targeted implementation technology. In this work we employed a Xilinx FPGA device. All calculations used in the developed modules are executed with fixed-point arithmetic using an appropriate and optimised data size. To get a simpler implementation and high-speed processing, mathematic algorithms are optimised in each part of the controller, and a new sector identification method is embedded. This results in a light FPGA implementation, less resource consumption, and rapid time response.

Simulation results show excellent performance of the developed controller design, where current harmonic compensation and unity power factor are highlighted. It indicates that FPGA-based implementation of DPC is an effective, flexible, and successful solution for SAPF control.

References

- Akagi, H. (2005). The state-of-the-art of active filters for power conditioning. In: *2005 European Conference on Power Electronics and Applications*. Dresden, 11-14 September 2005.
- Alonso-Martínez, J., Carrasco, J. E.-G. and Arnaltes, S. (2010). Table-Based Direct Power Control: A Critical Review for Microgrid Applications. *IEEE Transactions on Power Electronics*, 25(12), pp. 2949–2961.
- Anjana, P., Gupta, V., Tiwari, H., Gupta, N. and Bansal, R. (2016). Hardware Implementation of Shunt APF using Modified Fuzzy Control Algorithm with STM32F407VGT Microcontroller. *Electric Power Components and Systems*, 44(13), pp. 1530–1542.

- Baros, J., Sotola, V., Bilik, P., Martinek, R., Jaros, R., Danys, L. and Simonik, P. (2022). Review of Fundamental Active Current Extraction Techniques for SAPF. *Sensors*, 22(20), p. 7985.
- Benhamadouche, A. D., Djahli, F., Ballouti, A. and Sahli, A. (2019). FPGA-Based Hardware-in-the-Loop for Multi-Domain Simulation. *International Journal of Modeling, Simulation, and Scientific Computing*, 10(04), p. 1950020.
- Bouafia, A., Gaubert, J. P. and Chaoui, A. (2012). Direct Power Control Scheme Based on Disturbance Rejection Principle for Three-Phase PWM AC/DC Converter under Different Input Voltage. *Journal of Electrical Systems*, 8(4), pp. 367–383.
- Bouafia, A., Krim, F. and Gaubert, J.-P. (2009). Fuzzy-Logic-Based Switching State Selection for Direct Power Control of Three-Phase PWM Rectifier. *IEEE Transactions on Industrial Electronics*, 56(6), pp. 1984–1992.
- Dash, S. K. and Ray, P. K. (2017). Platform Specific FPGA Based Hybrid Active Power Filter for Power Quality Enhancement. *International Journal of Emerging Electric Power Systems*, 18(1), p. 20160143.
- Garcia-Cerrada, A., Pinzón-Ardila, O., Feliu-Batlle, V., Roncero-Sánchez, P. and García-González, P. (2007). Application of a Repetitive Controller for a Three-Phase Active Power Filter. *IEEE Transactions on Power Electronics*, 22(1), pp. 237–246.
- Hu, J., Shang, L., He, Y. and Zhu, Z. Q. (2011). Direct Active and Reactive Power Regulation of Grid-Connected DC/AC Converters using Sliding Mode Control Approach. *IEEE Transactions on Power Electronics*, 26(1), pp. 210–222.
- Jain, S. (2018). Control strategies of shunt active power filter. In: S. K. Dwivedi, S. Jain, K. K. Gupta, and P. Chaturvedi, eds., *Modeling and Control of Power Electronics Converter System for Power Quality Improvements*. Amsterdam: Elsevier, pp. 31–84.
- Karimi, S., Poure, P., Saadate, S. and Gholipour, E. (2008). FPGA-Based Fully Digital Controller for Three-Phase Shunt Active Filters. *International Journal of Electronics*, 95(8), pp. 805–818.
- Li, D., Wang, T., Pan, W., Ding, X. and Gong, J. (2021). A Comprehensive Review of Improving Power Quality using Active Power Filters. *Electric Power Systems Research*, 199, p. 107389.
- Mesbahi, N., Ouari, A., Abdeslam, D. O., Djamah, T. and Omeiri, A. (2014). Direct Power Control of Shunt Active Filter using High Selectivity Filter (HSF) under Distorted or Unbalanced Conditions. *Electric Power Systems Research*, 108, pp. 113–123.
- Mikkili, S. and Panda, A. K. (2018). *Power Quality Issues: Current Harmonics*. Boca Raton: CRC press.
- Monmasson, E., Idkhajine, L., Cirstea, M. N., Bahri, I., Tisan, A. and Naouar, M. W. (2011). FPGAs in Industrial Control Applications. *IEEE Transactions on Industrial Informatics*, 7(2), pp. 224–243.
- Montero, M. I. M., Cadaval, E. R. and Gonzalez, F. B. (2007). Comparison of Control Strategies for Shunt Active Power Filters in Three-Phase Four-Wire Systems. *IEEE Transactions on Power Electronics*, 22(1), pp. 229–236.
- Mulla, M. A., Chudamani, R. and Chowdhury, A. (2015). A Novel Control Method for Series Hybrid Active Power Filter Working Under Unbalanced Supply Conditions. *International Journal of Electrical Power and Energy Systems*, 64, pp. 328–339.
- Nian, H., Shen, Y., Yang, H. and Quan, Y. (2015). Flexible Grid Connection Technique of Voltage-Source Inverter under Unbalanced Grid Conditions based on Direct Power Control. *IEEE Transactions on Industry Applications*, 51(5), pp. 4041–4050.
- Noguchi, T., Tomiki, H., Kondo, S. and Takahashi, I. (1998). Direct Power Control of PWM Converter Without Power-Source Voltage Sensors. *IEEE Transactions on Industry Applications*, 34(3), pp. 473–479.
- Popescu, M., Bitoleanu, A. and Suru, V. (2012). A DSP-Based Implementation of the p-q Theory in Active Power Filtering under Nonideal Voltage Conditions. *IEEE Transactions on Industrial Informatics*, 9(2), pp. 880–889.
- Rodriguez-Andina, J. J., Moure, M. J. and Valdes, M. D. (2007). Features, Design Tools, and Application Domains of FPGAs. *IEEE Transactions on Industrial Electronics*, 54(4), pp. 1810–1823.
- Sharma, S., Verma, V. and Behera, R. K. (2019). Real-Time Implementation of Shunt Active Power Filter with Reduced Sensors. *IEEE Transactions on Industry Applications*, 56(2), pp. 1850–1861.
- Shu, Z., Guo, Y. and Lian, J. (2008). Steady-State and Dynamic Study of Active Power Filter with Efficient FPGA-Based Control Algorithm. *IEEE Transactions on Industrial Electronics*, 55(4), pp. 1527–1536.
- Singh, B., Al-Haddad, K. and Chandra, A. (1999). A Review of Active Filters for Power Quality Improvement. *IEEE Transactions on Industrial Electronics*, 46(5), pp. 960–971.
- Singh, B., Singh, B. N., Chandra, A. and Al-Haddad, K. (2000). DSP-Based Implementation of an Improved

- Control Algorithm of a Three-Phase Active Filter for Compensation of Unbalanced Non-Linear Loads. *European Transactions on Electrical Power*, 10(1), pp. 29–35.
- Sundaram, E. and Venugopal, M. (2016). On Design and Implementation of Three Phase Three Level Shunt Active Power Filter for Harmonic Reduction using Synchronous Reference Frame Theory. *International Journal of Electrical Power and Energy Systems*, 81, pp. 40–47.
- Sutikno, T., Jidin, A. and Idris, N. R. N. (2010). New Approach FPGA-Based Implementation of Discontinuous SVPWM. *Turkish Journal of Electrical Engineering and Computer Sciences*, 18(4), pp. 499–514.
- Vazquez, S., Marquez, A., Aguilera, R., Quevedo, D. E., Leon, J. I. and Franquelo, L. G. (2015). Predictive direct power control for grid connected power converters with DC-link voltage dynamic reference design. In: *2015 IEEE International Conference on Industrial Technology (ICIT)*. Seville, 17-19 March 2015.
- Yan, S., Yang, Y., Hui, S. Y. and Blaabjerg, F. (2021). A Review on Direct Power Control of Pulsewidth Modulation Converters. *IEEE Transactions on Power Electronics*, 36(10), pp. 11984–12007.
- Yu, K., Yang, Z., Li, Y., Yi, H., Wang, F. and Zhuo, F. (2020). Three-phase three-level shunt APF control system based on multi-task parallel MCU. In: *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*. New Orleans, 15-19 March 2020.
- Zahira, R. and Fathima, A. P. (2012). A Technical Survey on Control Strategies of Active Filter for Harmonic Suppression. *Procedia Engineering*, 30, pp. 686–693.
- Zhi, D., Xu, L. and Williams, B. W. (2009). Improved Direct Power Control of Grid-Connected DC/AC Converters. *IEEE Transactions on Power Electronics*, 24(5), pp. 1280–1292.